

CLAIMS:

We claim:

1. A semiconductor device comprising:
5 an isolation layer formed in a semiconductor substrate to define an active region;
a gate pattern formed in the active region;
source/drain regions formed in the active region at both sides of the gate pattern;
sidewall spacers formed on sidewalls of the gate pattern;
a blocking insulation layer formed on the isolation layer and on a portion of the active
10 region neighboring the isolation layer; and
a silicide layer formed on the source/drain regions between the blocking insulation
layer and the sidewall spacers and having a boundary aligned to edges of the blocking
insulation layer and the sidewall spacer.

15 2. The semiconductor device of claim 1, wherein the sidewall spacer comprises:
an inner spacer having an L-shaped cross-section that is formed on the sidewall of the
gate pattern and on the active region neighboring the gate pattern; and
an outer spacer having a curved sidewall that is formed on the inner spacer.

20 3. The semiconductor device of claim 1, wherein the isolation layer includes a
dent at the region neighboring the active region, and
wherein the blocking insulation layer is formed on the dent.

25 4. The semiconductor device of claim 1, further comprising:
a silicide layer formed on a top surface the gate pattern.

5. A method of fabricating semiconductor devices comprising:
forming a isolation layer in a semiconductor substrate to define an active region;
forming a gate pattern on the active region;
implanting impurities into the active region at both sides of the gate pattern;
30 forming a spacer insulation layer on a surface of the semiconductor substrate with the
gate pattern, the spacer insulation layer having a first region between the isolation layer and
the gate pattern, wherein the closer the first region lies to the gate pattern, the thinner it
becomes;

anisotropically etching the spacer insulation layer to form a sidewall spacer on a sidewall of the gate pattern, and to leave a blocking insulation layer on the isolation layer and on a portion of the active region neighboring the isolation layer; and

5 applying a silicidation process to the semiconductor substrate to form a silicide layer on a source/drain region between the blocking insulation layer and the sidewall spacer, the silicide layer having a boundary aligned to the edge of the blocking insulation layer and a boundary aligned to the edge of the the sidewall spacer.

10 6. The method of claim 5, wherein forming the spacer insulation layer comprises: stacking a silicon nitride layer and a silicon oxide layer, wherein the first region includes at least one of the silicon nitride layer and the silicon oxide layer.

15 7. The method of claim 6, wherein anisotropically etching the spacer insulation layer to form the sidewall spacer comprises:

15 anisotropically etching the silicon oxide layer to form an outer spacer having a curved sidewall on a side of a gate electrode; and
etching the silicon nitride layer using the outer spacer as an etch stop layer to form an inner spacer having an L-shaped cross-section between the outer spacer and the gate pattern.

20 8. The method of claim 5, wherein forming the spacer insulation layer comprises: conformally forming a silicon nitride layer on the semiconductor substrate; and forming a silicon oxide layer on the silicon nitride layer, wherein the first region comprises the silicon oxide layer.

25 9. The method of claim 8, wherein anisotropically etching the spacer insulation layer comprises:

anisotropically etching the silicon oxide layer to form an outer spacer on a sidewall of the gate pattern and to form a blocking oxide layer on the isolation layer and on a portion of the active region neighboring the isolation layer; and

30 etching the silicon nitride layer using the outer spacer and the blocking oxide layer as an etch mask to form an inner spacer interposed between the outer spacer and the gate pattern and to form a blocking nitride layer under the blocking oxide layer.

10. The method of claim 5, wherein forming the spacer insulation layer comprises: forming a silicon nitride layer on the semiconductor substrate, wherein the first region comprises the silicon nitride layer; and
conformally forming a silicon oxide layer on the silicon nitride layer.

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11. The method of claim 10, wherein anisotropically etching the spacer insulation layer comprises:

anisotropically etching the silicon oxide layer to form an outer spacer on the sidewall of the gate pattern; and

10 etching the silicon nitride layer using the outer spacer as an etch mask to form a blocking nitride layer on the isolation layer and on a portion of the active region neighboring the isolation layer.

12. The method of claim 5, wherein anisotropically etching the spacer insulation layer comprises:

etching the spacer insulation layer on the active region neighboring the gate pattern is etched at a faster rate than the spacer insulation layer on the active region neighboring the field insulation layer.